بسم الله الرحمن الرحيم

Republic of Iraq

The Ministry Of Higher Education

& Scientific Research

University: Baghdad University
College: College of Science for women
Department: Computer Dept.
Stage: Third/ First Semester
Lecturer name: Raja 'a Mureeh Mohammed

Qualification: Master in Computer Science

Place of work: College of Science for women/ Computer Dept.

Syllabus Form

Instructor Name	Raja 'a Mureeh Mohammed				
E-mail	Rajaa007700@yahoo.com				
Course Title	Advanced Computer Architecture				
Course Coordinator					
Course Objectives	The objective of the course is to provide in-depth coverage of current and emerging trends in computer architectures, focusing on performance and the hardware/software interface. And To enable a better understanding of the concepts, hands-on assignments are used to explore issues in multiprocessors architecture systems.				
Course Description	1. Getting the knowledge of the trends in computer architectures. 2. Understand the Instruction Level Parallelism (ILP). 3. Understand Multiprocessors and thread-level parallelism. 4. Understand Memory hierarchy design.				
Textbook	Computer Architecture, by Hennessy, J and Patterson, D. , 4'th Edition,Morgan Kaufmann Publishers, 2007				
References	Advanced Computer Architecture, by Kai Hwang, 1'st Edition ,McGrow- Hill,1993				
Course Assessments	Term Tests	Laboratory	Quizzes	Project	Final Exam
	30%	-	10%	-	60%
General Notes					

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ourse Weekly Outline

Week	Date	Topes Covered	Lab. Experiment Assignments	Notes
1		Fundamental of computer design		
2		Trends in Technology		
3		Dependability		
4		Amdahl's low		
5		Instruction Level Parallelism (ILP) Concept and Challenges		
6		Basic Compiler Technologies for Exploiting ILP		
7		Exam		
8		Overcoming Data Hazards with Dynamic Scheduling		
9		Multiprocessors and thread-level parallelism		
10		Multiprocessors and		

		thread-level parallelism		
11		Models of communication and memory architecture		
12		Challenges of parallel processing		
13		What is multiprocessor cache coherence		
14		Exam		
15		Memory hierarchy design		
16		Eleven advance optimization of cache performance		

Instructor Signature: **Dean Signature:**